PVP 20

Code: 20EE4501E

III B.Tech - I Semester – Regular Examinations - DECEMBER 2022

COMPUTER ORGANIZATION & ARCHITECTURE
(ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
UNIT-I					
1	a)	Compare between Harvard and Von-Neumann based Computer Architectures.	L2	CO1	5 M
	b)	Develop a 4-bit arithmetic circuit using four full adders.	L3	CO2	9 M
OR					
2	a)	List out the microoperations required for the following tasks: i) Fetch data from memory to a processor register ii) Transfer data from a processor register to another register iii) Transfer data immediately to a processor register	L3	CO2	9 M
	b)	Demonstrate the hardware implementation of a 4-bit combinational shifter.	L3	CO2	5 M

UNIT-II					
3	a)	Explain how an instruction cycle can be fragmented into different phases and the role of each phase with the help of neat diagram.	L2	CO1	7 M
	b)	Develop a hardware circuit to fetch the address of a next instruction for a processor which executes three different types of instructions namely, memory reference instructions, register reference instructions and branch instructions.	L3	CO3	7 M
OR					
4	a)	Illustrate the various phases involved in the execution of a interrupt cycle.	L3	CO2	7 M
	b)	Demonstrate the common bus system of a basic computer.	L3	CO3	7 M
UNIT-III					
5	a)	It is required to perform OR operation between two numbers. Suggest and explain suitable addressing modes to fetch the data from source memory locations and store the data into destination locations to accomplish the above task.	L3	CO3	7 M
	b)	Analyze and design a stack memory to be connected to a computer.	L3	CO3	7 M
OR					
6	a)	Analyze the role of stack memory in the execution of a Interrupt service procedure call when an interrupt occurs in the main program and return to the main program from interrupt service routine.	L3	CO3	7 M

	b)	Compare between the various types of instructions employed in the design of a Complex Instruction Set Computer. (Hint: One byte, Two byte and Three byte Instructions).	L3	CO3	7 M
		UNIT-IV			
7	a)	Develop an efficient architecture to design a 4-bit signed magnitude subtractor.	L3	CO4	7 M
	b)	Evaluate the search time involved in Direct, Set-Associative and fully associative CACHE memory mapping techniques and show that the set associative mapping is efficient mapping technique over other techniques.	L4	CO4	7 M
		OR			
8	a)	On behalf of Government of India, it has been announced to distribute 36KGs of food grains in a period of 6 months during COVID19 Pandemic. If certain village has a population of 492 people, compute the quantity of food grains required employing an efficient binary arithmetic architecture.	L3	CO4	7 M
	b)	Illustrate the diagram of memory hierarchy and explain.	L3	CO2	7 M
		UNIT-V			
9	a)	Compare between Isolated I/O and Interrupt driven I/O based data transfer mechanism.	L2	CO1	4 M
	b)	It is required to transfer a data of 512MB from hard disk drive of a computer to flash drive. Suggest a suitable method and the necessary steps required to accomplish the required task with neat diagrams.	L4	CO4	10 M

		OR			
10	a)	Analyze and explain how Strobed I/O based data transfer can be made with the help of neat timing diagrams. Explain how a keyboard can be connected to a processor employing strobed I/O based data transfer.	L4	CO4	10 M
	b)	Analyze and explain how Pipelined processor based architectures improves the performance of the system.	L2	CO1	4 M